

AMENDMENTS TO THE DRAWINGS

FIG. 1 and FIG. 4 have been amended by replacing the word “STANDARD” in element number 2 with the word “REFERENCE”. Replacement sheets for FIG. 1 and FIG. 4 are included in Appendix C.

REMARKS

By this amendment, the specification has been amended to change the phrase "standard voltage" to the phrase "reference voltage" where it was found in the specification. Amendments to the specification are reflected in the substitute specification submitted herewith. A clean version of the substitute specification is included as Appendix A. A marked up version of the substitute specification showing the changes is included as Appendix B. The substitute specification contains no new matter. The original specification as filed is included in Appendix D.

FIG. 1 and FIG. 4 have been amended by replacing the word "STANDARD" in element number 2 with the word "REFERENCE". Replacement sheets for FIG. 1 and FIG. 4 are included in Appendix C.

Favorable consideration is respectfully requested.

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DESCRIPTION

SWITCHING REGULATOR AND METHOD FOR SWITCHING
OUTPUT VOLTAGE THEREOF

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TECHNICAL FIELD

The present invention generally relates to a
switching regulator that can change the output voltage used
in portable devices, and especially to a switching regulator
10 for lowering an overshoot of the output voltage when
increasing the output voltage, and a method for switching the
output voltage of the switching regulator.

BACKGROUND ART

15 In recent years, the saving energy has become
desirable from the point of view of environmental operations.
In devices such as a cell phone, a digital camera and the
like wherein a battery is used, reducing the electric power
consumed in the devices has become more important from the
20 view of increasing the service life of the battery. For this
purpose, as for the power supply circuit, non-insulated step-
down type switching regulators with high efficiency and
reduced size in which an inductor is used are in wide use
(hereinafter, referred to as switching regulators). The
25 switching regulators are highly efficient at rated loads.

However, since the consumption of electric current by the switching regulators themselves is comparatively large, the efficiency of the devices becomes extremely low when the devices are in a light-load drive mode such as a stand-by mode, a sleep mode and the like.

In order to improve the efficiency even if the devices are in the light-load drive mode, Japanese Laid-Open Patent Application No.2002-300774 provides a method for reducing the electric power consumed in the switching regulator by switching PWM control to PFM control in the light-load drive mode so as to lower the switching frequency.

Fig.5 is a schematic circuit diagram illustrating an example of the switching regulator.

In Fig.5, a switching regulator 100 includes a PWM control circuit 101 and a PFM control circuit 102. The switching regulator 100 further includes a switching element 103 driven in the PWM control circuit 101 and another switching element 104 driven in the PFM control circuit 102.

In the normal operating mode, the PFM control circuit 102 stops operations. The PWM control circuit 101 operates so as to control switching on and off the switching element 103. In the light-load drive mode, the PWM control circuit 101 stops operating. The PFM control circuit 102 operates so as to control switching on and off the switching element 104.

Since a large amount of the electricity flows in the switching element 103 which is used when performing the PWM control, the size of the element 103 is increased so as to lower the on-resistance. However, this causes an increase
5 of the gate capacitance since the element 103 size becomes large.

The loss of the switching regulator in a case where the electric current is supplied to the load (hereinafter, referred to as the load electric current)
10 consists mostly of loss owing to the on-resistance of the switching element 103. When the load electric current is small, the loss of the switching regulator consists mostly of a loss owing to the charging and discharging of the gate capacitance of the switching element 103.

15 Accordingly, the switching element 104 is reduced in size to keep the gate capacitance small even though the on-resistance of the switching element 104 is large. The efficiency of the switching regulator is improved thereby.

Japanese Laid-Open Patent Publication No.2002-
20 300774 discloses such a switching regulator.

However, there is a problem of generating overshoot in the output voltage as shown in Fig.6, when the output voltage of the switching regulator is enabled to change from the low voltage to the high voltage. In addition,
25 there is another problem that the overshoot becomes larger

when the switching element with a high on-resistance is changed to a switching element with a low on-resistance at the same time as changing the output voltage.

Moreover, in the light-load drive mode in which
5 the load electric current is small, the load circuits such as a CPU using the switching regulator 100 as a power supply for operation often stops the operation, that is, the load circuits are in the sleep mode or in the stand-by mode. In such a light-load drive mode, the operating voltage of the
10 load circuits can often be smaller than the operation voltage in the normal drive mode. Accordingly, it is normal that the output voltage of the switching regulator is lowered so as to lower the load electric current.

However, in a case of shifting the drive mode from
15 the light-load drive mode to the normal drive mode, when switching the control mode of the switching regulator from the PFM control to the PWM control and simultaneously changing the output voltage from the low voltage to the high voltage, the overshoot voltage is generated in the output
20 voltage as described above. Accordingly, there is a risk of causing failure in the CPU and the other circuits.

DISCLOSURE OF THE INVENTION

The present invention provides a switching
25 regulator and a method for switching the output voltage

thereof that can realize lowering the overshoot generated when raising the output voltage in shifting from the light-load drive mode to the normal drive mode and that substantially obviates one or more problems caused by the
5 limitations and disadvantages of the related art.

A preferred embodiment of the present invention provides a switching regulator converting an input voltage to a predetermined voltage and outputting the predetermined voltage to a load through an output terminal. The switching
10 regulator includes a first switching element including a first control electrode performing switching according to a control signal input to the first control electrode and controlling outputting the input voltage, a second switching element including a second control electrode having
15 capacitance larger than the capacitance of the first control electrode of the first switching element and an on-resistance smaller than the on-resistance of the first switching element. The second switching element performs switching according to a control signal input to the second control electrode and
20 controls outputting the input voltage. The switching regulator further includes a control switching circuit part performing one of a PWM control on both of the first switching element and the second switching element and a PFM control only on the second switching element according to an
25 operating mode so that a voltage output from the output

terminal is the predetermined voltage, and a smoothing circuit smoothing a voltage output from each of the first switching element and the second switching element and outputting the smoothed voltage to the output terminal. When
5 a first operating mode in which the PFM control is performed and the voltage from the output terminal becomes a first voltage is shifted to a second operating mode in which the PWM control is performed and the voltage from the output terminal becomes a second voltage larger than the first
10 voltage, the control switching circuit part increases the voltage from the output terminal stepwise progressively from the first voltage to the second voltage while performing the PWM control.

According to at least one of the embodiments of
15 the present invention, a method for switching an output voltage of a switching regulator is provided. The switching regulator includes an input terminal, an output terminal, a load, a first switching element including a first control electrode performing switching according to a control signal
20 input to the first control electrode and controlling outputting an input voltage and a second switching element including a second control electrode having capacitance larger than the capacitance of the first control electrode of the first switching element and an on-resistance smaller than
25 the on-resistance of the first switching element. The second

switching element performs switching according to a control signal input to the second control electrode and controls outputting the input voltage. The switching regulator is enabled to change the output voltage so as to convert the

5 input signal input from the input terminal into a predetermined voltage and to output the predetermined voltage to the load via the output terminal by performing one of a PWM control on both of the first switching element and the second switching element and a PFM control only on the second

10 switching element according to an operating mode, the method comprising a step of increasing the voltage from the output terminal stepwise progressively from the first voltage to the second voltage while performing the PWM control when a first operating mode in which a PFM control is performed and the

15 voltage from the output terminal becomes a first voltage is shifted to a second operating mode in which PWM control is performed and the voltage from the output terminal becomes a second voltage larger than the first voltage.

According to the above described switching

20 regulator, when the first operating mode in which the PFM control is performed and the output voltage from the output terminal becomes the predetermined first voltage is shifted to the second operating mode in which the PWM control is performed and the output voltage from the output terminal

25 becomes the second voltage larger than the first voltage, the

PWM control is performed and the output voltage from the output terminal is gradually increased from the first voltage to the second voltage. Accordingly, overshoot voltage which is generated when increasing the output voltage is reduced so that the output voltage can be switched without being influenced by the overshoot. Moreover, the switching elements which are fitted to each of the PWM control and the PFM control are adopted so as to increase the efficiency both in the PWM control and the PFM control.

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BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 is a configuration example of a switching regulator according to the first embodiment of the present invention.

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Fig.2 is a timing chart illustrating an operating example of shifting from a light-load drive mode to a normal drive mode.

Fig.3 is a flowchart illustrating an operating example of a control circuit 10 shown in Fig.1.

20

Fig.4 is another configuration example of the switching regulator according to the first embodiment of the present invention.

Fig.5 is a schematic circuit diagram illustrating an example of a conventional switching regulator.

25

Fig.6 is a view illustrating a waveform example of

the output voltage shown in Fig.5.

BEST MODE FOR CARRYING OUT THE INVENTION

Next, a detailed description is given of preferred
5 embodiments shown in the accompanying drawings of the present
invention.

(First Embodiment)

Fig.1 is a configuration example of a switching
regulator 1 according to the first embodiment of the present
10 invention.

In Fig.1, an output voltage variable switching
regulator is provided for generating a predetermined voltage
from an input voltage Vdd input to the Vdd terminal which is
an input terminal from a DC voltage BAT and outputting the
15 predetermined voltage as an output voltage Vo from an output
terminal OUT to a load 20.

The switching regulator 1 includes a first
switching element M1 comprising a PMOS transistor performing a
switching operation for controlling outputting the input
20 voltage Vdd, another switching element M2 for synchronous
rectification comprising an NMOS transistor, an inductor L1
and a condenser C1 comprising a smoothing circuit, and output
voltage detecting resistors R1 and R2 for dividing the output
voltage Vo so as to generate and output a divided voltage VFB.

25 Moreover, the switching regulator 1 further

includes a ~~standard~~reference voltage generation circuit 2 comprising a D/A converter generating and outputting a ~~standard~~reference voltage V_{ref} according to an input voltage setting signal V_S , an error amplifying circuit 3 comparing the
5 divided voltage V_{FB} with the ~~standard~~reference voltage V_{ref} and outputting an output signal Err according to the voltage comparison result, and a PWM control circuit 4 controlling switching of the first switching element M1 and the second switching element M2 for synchronous rectification by
10 performing PWM control on the first switching element M1 and the second switching element M2 for synchronous rectification according to the output signal Err from the error amplifying circuit 3.

The switching regulator 1 moreover includes a
15 second switching element M3 comprising a CMOS transistor smaller than the CMOS transistor of the first switching element M1 in which the second switching element M3 controls outputting the input voltage V_{dd} input to the V_{dd} terminal, a PFM control circuit 5 performing PFM control on the second
20 switching element M3 according to the output signal Err of the error amplifying circuit 3, an oscillation circuit OSC generating a triangular wave signal TW of a predetermined frequency and outputting the triangular wave signal TW to each of the PWM control circuit 4 and the PFM control circuit 5.
25 The second switching element M3 has an on-resistance larger

than the on-resistance of the first switching element M1 and a gate capacitance smaller than the gate capacitance of the first switching element M1.

The switching regulator 1 further includes a first
5 switch SW1 outputting one of a signal PD output from the PWM control circuit 4 to a gate of the first switching element M1 and a signal Spf output from the PFM control circuit 5, to a gate of the second switching element M3 according to the switching signal FWS directing switching the operating mode.
10 In addition, the switching regulator 1 includes an overcurrent protection circuit 6 performing the steps of detecting the electric current flowing into the inductor L1, determining whether the detected electric current is over a predetermined value, and switching off the first switching element M1 and
15 the switching element M2 for synchronous rectification for the PWM control circuit 4 when the detected electric current is over the predetermined value.

The switching regulator 1 furthermore includes a dummy load 7 which is a pseudo load in which a predetermined
20 electric current flows, a second switch SW2 controlling the connection of the dummy load 7 to the output terminal OUT, and a control circuit 10 generating and outputting the voltage setting signal VS and the switching signals FWS and DLS according to a predetermined sequence. It should be noted
25 that the ~~standard~~reference voltage generation circuit 2, the

error amplifying circuit 3, the PWM control circuit 4, the PFM control circuit 5, the oscillation circuit OSC, the resistors R1 and R2, the first and second switches SW1 and SW2, and the control circuit 10 comprise a control switching circuit part.

5 In addition, the ~~standard~~reference voltage generation circuit 2, the error amplifying circuit 3, the PWM control circuit 4, the oscillation circuit OSC, and the resistors R1 and R2 comprise a PWM control circuit part. The ~~standard~~reference voltage generation circuit 2, the error amplifying circuit 3,

10 the PFM control circuit 5, the oscillation circuit OSC, and the resistors R1 and R2 comprise a PFM control circuit part. The first switch SW1 comprises a switching circuit part. The control circuit 10 and the second switch SW2 comprise a control circuit part. Further, the switching element M2 for

15 synchronous rectification, the inductor L1 and the condenser C1 comprise a smoothing circuit part.

The PWM control circuit 4 includes PWM circuit 11 generating and outputting a pulse signal Spw from the output signal Err of the error amplifying circuit 3 and the

20 triangular wave signal TW of the oscillation circuit OSC so as to perform the PWM control, and a drive circuit 12 generating and driving the control signal PD for controlling switching the first switching element M1 according to the pulse signal Spw from the PWM circuit 11 and a control signal ND for

25 controlling switching the switching element M2 for synchronous

rectification.

It should be noted that in the switching regulator 1, each part excluding the inductor L1 and the condenser C1 is integrated in an IC. The IC includes terminals Vdd, LX, ECO, FB and GND. The Vdd terminal is provided as an input terminal of the switching regulator 1. The GND terminal is connected to ground voltage.

The DC battery BAT is connected between the Vdd terminal and the GND terminal. The input voltage Vdd is input from the DC battery BAT to the Vdd terminal. A load 20 is connected between the output terminal OUT and ground. The first switching element M1 and the second switching element M3 are connected in parallel between the Vdd terminal and the LX terminal. The switching element M2 for synchronous rectification is connected between the LX terminal and ground. In addition, the inductor L1 is connected between the LX terminal and the output terminal OUT. The condenser C1 is connected between the output terminal OUT and ground. The connection between the inductor L1 and the condenser C1 is connected to the FB terminal. The resistors R1 and R2 are connected in series between the FB terminal and ground.

A part connecting the resistors R1 and R2 is connected to an inverting input terminal of the error amplifying circuit 3. The ~~standard~~reference voltage Vref is input to a non-inverting input terminal of the error

amplifying circuit 3. The output signal Err of the error
amplifying circuit 3 is output to each of the PFM control
circuit 5 and an inverting input terminal of a comparator
comprising the PWM circuit 11. The triangular wave signal TW
5 from the oscillation circuit OSC is output to each of the PFM
control circuit 5 and a non-inverting input terminal of the
PWM circuit 11. The pulse signal Spw from the PWM circuit 11
is output to the drive circuit 12. The pulse signal Spf
output from the PFM control circuit 5 is input to the PFM
10 terminal of the first switch SW1.

The drive circuit 12 outputs the control signal PD
for controlling switching the first switching element M1 to
each of the gate of the first switching element M1 and the PWM
terminal of the first switch SW1. The drive circuit 12
15 further outputs the control signal ND for controlling
switching the switching element M2 for synchronous
rectification to the gate of the switching element M2 for
synchronous rectification. A COM terminal of the first switch
SW1 is connected to the gate of the second switching element
20 M3. The overcurrent protection circuit 6 monitors the
electric current flowing into the LX terminal and outputs the
monitoring result to the drive circuit 12. In addition, the
switching signal FWS from the control circuit 10 is input to
each of the PFM control circuit 5, the overcurrent protection
25 circuit 6, the PWM circuit 11, the drive circuit 12 and the

first switch SW1. Further, the second switch SW2 and the dummy load 7 are connected in series between the FB terminal and ground. The switching signal DLS is input from the control circuit 10 to the second switch SW2. The second
5 switch SW2 performs switching according to the switching signal DLS.

In the above described configuration, the switching signal FWS is provided for switching between the normal drive mode and the light-load drive mode with a consumption current
10 smaller than the normal drive mode. The control circuit 10 generates and outputs the switching signal FWS according to a control signal input to the ECO terminal from the outside. It should be noted that the control circuit 10 can output the switching signal FWS so as to switch to the light-load drive
15 mode when the electric current flowing in the load 20 is measured and found out to be under a predetermined value. Or the control circuit 10 can output the switching signal FWS when the device including the switching regulator 1 shifts to the stand-by mode. It should be noted that the light-load
20 drive mode is the first operating mode, while the normal drive mode is the second operating mode.

First, a description is given of a case in which the switching signal FWS selects the normal drive mode. In this case, the PFM control circuit 5 stops operations and cuts
25 the consumption electric current in the PFM control circuit 5

or reduces the consumption of electric current to the minimum. Simultaneously, the PWM circuit 11, the drive circuit 12 and the overelectric current protection circuit 6 operate. The switching regulator 1 operates as a switching regulator of synchronous rectification type. Further, the first switch SW1 is switched so that the COM terminal can be connected to the PWM terminal. Then, the control signal PD from the drive circuit 12 is input to the gate of the second switching element M3.

10 According to the above description, each of the first and second switching elements M1 and M3 performs a switching operation. When the first and second switching elements M1 and M3 are in an ON state, an electric current is supplied to the inductor L1. At this time, the switching
15 element M2 for synchronous rectification is in an OFF state. When each of the first and second switching elements M1 and M3 are in the OFF state, the switching element M2 for synchronous rectification is in the ON state. Then, the energy stored in the inductor L1 is transferred through the switching element
20 M2 for synchronous rectification. The electric current generated at this time is smoothed in the condenser C1 and output via the output terminal OUT to the load 20.

 Moreover, the output voltage V_o output from the output terminal OUT is divided into the divided voltage VFB in
25 the output voltage detecting resistors R1 and R2. Then, the

divided voltage VFB is input to the inverting input terminal of the error amplifying circuit 3. Since the standard reference voltage Vref is input to the non-inverting input terminal of the error amplifying circuit 3, the voltage
5 difference between the divided voltage VFB and the standard reference voltage Vref is amplified in the error amplifying circuit 3 and output to the inverting input terminal of the PWM circuit 11. The triangular wave signal TW from the oscillation circuit OSC to is input the non-inverting
10 input terminal of the PWM circuit 11. The PWM circuit 11 outputs the pulse signal Spw on which the PWM control is performed to the drive circuit 12.

As the output voltage Vo of the switching regulator 1 increases, the output signal Err of the error amplifying
15 circuit 3 is reduced. The duty cycle of the pulse signal Spw from the PWM circuit 11 is also reduced. As a result, the period where the first and second switching elements M1 and M3 are in the ON state is reduced. The output voltage Vo of the switching regulator 1 is controlled so as to be lowered. When
20 the output voltage Vo of the switching regulator 1 becomes small, operations reverse to the above described operations are performed. Accordingly, the output voltage Vo of the switching regulator 1 is controlled to be constant.

The overcurrent protection circuit 6 compares the
25 voltage drops of the respective switching elements M1 and M3

with the predetermined voltage when the switching elements M1 and M3 are in the ON state. When the voltage drops become greater than the predetermined voltage, the overcurrent protection circuit 6 outputs a predetermined signal so as to
5 stop the operation of the drive circuit 12. When the drive circuit 12 stops operating, the overcurrent protection circuit 6 sets the control signal PD to a high level and the control signal ND a low level so that the first and second switching elements M1 and M3 and the switching element M2 for
10 synchronous rectification can be switched off. Accordingly, the supply of the output electric current from the output terminal OUT is stopped.

Next, a description is given of a case where the switching signal FWS selects the light-load drive mode. In
15 this case, the PFM control circuit 5 operates, while the PWM circuit 11, the drive circuit 12, and the overcurrent protection circuit 6 stop operations. The consumption electric currents thereof are cut or reduced to the minimum. Moreover, the first switch SW1 is switched so that the COM
20 terminal can be connected to the PFM terminal. The pulse signal Spf from the PFM control circuit 5 on which the PFM control is performed is input to the gate of the second switching element M3. The second switching element M3 performs switching operations according to the pulse signal
25 Spf from the PFM control circuit 5. At this time, since the

drive circuit 12 stops the operation, the switching element M2 for synchronous rectification remains in the OFF state.

Accordingly, the energy stored in the inductor L1 is transferred through a parasite diode D1 connected between the source and drain of the switching element M2 for synchronous rectification.

Here, a description is given of the operation when the light-load drive mode is shifted to the normal drive mode with reference to a timing chart shown in Fig.2 and a

flowchart shown in Fig.3. It should be noted that S1 through S7 shown in Fig.2 corresponds to S1 through S7 shown in Fig.3.

In Step S1, since the light-load drive mode is selected, the control circuit 10 sets the standardreference voltage Vref of the standardreference voltage generation circuit 2 by sending the voltage setting signal VS so that the output voltage Vo equals the first voltage Vol which is the predetermined voltage. Further, the control circuit 10 directs the switching regulator 1 to perform the PFM control with the switching signal FWS, and to switch off the second switch SW2 with the switching signal DLS.

Next, in step S2, with the switching signal FWS, the control circuit 10 directs the switching regulator 1 to perform the PWM control. Then, in step S3, the control circuit 10 changes the standardreference voltage Vref output with the voltage setting signal VS so as to increase the

output voltage V_o of the switching regulator 1 gradually. At this time, the control circuit 10 adjusts the output voltage V_o by changing the standardreference voltage V_{ref} output from the standardreference voltage generation circuit 2. The
5 standardreference voltage generation circuit 2 comprises a D/A converter.

The standardreference voltage generation circuit 2 generates and outputs a voltage according to the combination of bits of the voltage setting signal VS comprising plural
10 bits input from the control circuit 10. The control circuit 10 directs the switching regulator 1 to perform the PWM control, and then, outputs the voltage setting signal VS to the standardreference voltage generation circuit 2 so as to increase the output voltage V_o by αV . It should be noted
15 that the overshoot voltage is generated as a component of the output voltage at this time. However, the change of the output voltage V_o , i.e., αV is very small, and thus, the overshoot voltage is also small. Accordingly, a defect is not generated.

20 Next, in step S4, the control circuit 10 determines whether the voltage setting signal VS sets the standardreference voltage V_{ref} so that the output voltage V_o can be equal to the second voltage V_{o2} which is the predetermined voltage larger than the first voltage V_{o1} .
25 When the voltage setting signal VS contains the data which

set the ~~standard~~reference voltage V_{ref} so that the output voltage V_o can be equal to the predetermined second voltage V_{o2} (Yes in step S4), then the operation proceeds step S5. On the contrary, in step S4, if the voltage setting signal V_S contains data which set the ~~standard~~reference voltage V_{ref} so that the output voltage V_o is less than the second voltage V_{o2} (No in step S4), then, the operation returns to step S3. In other words, in steps S3 and S4, the output voltage V_o of the switching regulator 1 is gradually increased from the first voltage V_{o1} to the second voltage V_{o2} . Whenever the predetermined period elapses, the combination of the bits of the voltage setting signal V_S is changed and the output voltage V_o is increased by αV . As shown in step S4, when the output voltage V_o reaches the second voltage V_{o2} , the combination of the bits of the voltage setting signal V_S is stored and the output voltage V_o is fixed equal to the second voltage V_{o2} .

The voltage amplification α of the output voltage increased at one step is determined by the voltage difference between the first voltage V_{o1} and the second voltage V_{o2} and by a number of bits of the D/A converter comprising the ~~standard~~reference voltage generation circuit 2 so as to prevent the overshoot voltage from affecting the load 20. For example, when the voltage amplification α is set approximately 20 mV, the voltage amplification α is fixed.

Accordingly, as the voltage difference between the first voltage Vo1 and the second voltage Vo2 becomes larger, the number of steps for reaching the second voltage Vo2 is increased. It should be noted that in Fig.2, when the output
5 voltage Vo is the first voltage Vo1, the ~~standard~~reference voltage Vr is assigned Vr1. When the output voltage Vo is the second voltage Vo2, the ~~standard~~reference voltage Vr is assigned Vr2.

Next, in step S5, the control circuit 10 outputs
10 the switching signal DLS to switch the second switch SW2 into the conductive state. Accordingly, the second switch is switched on so that the dummy load 7 can be connected between the output terminal OUT and ground.

Here, a description is given of the reason why the
15 dummy load is connected.

When the control of the switching regulator 1 is switched from the PFM control to the PWM control, the load 20 is still not in the normal drive mode, since the electric current flowing into the load 20 is substantially the same as
20 the light-load drive mode. Thus, the electric current is extremely low. As above described, when the PFM control is switched to the PWM control in a state where the electric current flowing into the load 20 is substantially zero, the PWM circuit 11 performs abnormal operations such as a burst
25 oscillation immediately after switching the control. Thus,

the output voltage V_o becomes unstable.

It should be noted that while increasing the output voltage V_o , the charging electric current flows in the condenser C_1 connected to the output terminal OUT so as to prevent the PWM circuit 11 from performing abnormal operations such as the burst oscillation. However, after the output voltage V_o becomes equal to the second voltage V_{o2} , the PWM circuit 11 performs an abnormal operation. Thus, the output voltage V_o becomes unstable. In order to avoid the abnormal operations, after the output voltage V_o becomes equal to the second voltage V_{o2} , the dummy load 7 is connected to the output terminal OUT until the PWM circuit 11 performs stable operations. As for the timing of connecting the dummy load 7, the dummy load 7 can be connected immediately after switching to the PWM control. However, as described above, since abnormal operations are prevented while increasing the output voltage V_o , it is desirable to connect the dummy load 7 immediately after the output voltage V_o becomes equal to the second voltage V_{o2} .

The dummy load 7 can be connected starting immediately after switching to the PWM control and until the output voltage V_o reaches the second voltage V_{o2} . However, in this case, extra electricity is consumed by the electric current flowing into the dummy load 7 from when the dummy load 7 is connected until the output voltage reaches the

second voltage V_{o2} .

Next, in step S6, the control circuit 10 maintains the dummy load 18 connected for a predetermined period longer than the period needed for the PWM control to be normally performed. In step S7, after the predetermined period has elapsed, with the switching signal DLS, the second switch SW2 is switched off so as to terminate the flow. Accordingly, the operation of shifting the light-load drive mode to the normal drive mode is completed.

It should be noted that a flywheel diode D2 can be used as a substitute for the switching element M2 for synchronous rectification shown in Fig.1. The configuration of this case is shown in Fig.4. In Fig.4, the same reference numbers are assigned to the same or substantially the same components shown in Fig.1. Fig.4 shows the configuration example in which the flywheel diode D2 is disposed outside of the IC. When a diode such as a PN junction-type suited to integration is used as the flywheel diode D2, the flywheel diode D2 is provided inside of the IC.

Moreover, according to the description above, when increasing the output voltage V_o from the first voltage V_{o1} to the second voltage V_{o2} , the output voltage V_o is evenly and gradually increased at intervals of αV . The present invention is not limited to this; the output voltage V_o can be increased gradually from the first voltage V_{o1} to the

second voltage V_{o2} whether evenly and unevenly.

Accordingly, the switching regulator according to the first embodiment of the present invention switches the PFM control to the PWM control where the output voltage V_o is the first voltage V_{o1} , when the light-load drive mode is shifted to the normal drive mode. Then, the output voltage V_o is gradually increased little by little. Therefore, the overshoot generated when increasing the output voltage V_o can be controlled to be small. Thus, the output voltage V_o can be switched without being influenced by the overshoot. Moreover, the dummy load is connected so as to prevent an abnormal operation such as a burst oscillation immediately after the PFM control is shifted to the PWM control.

According to at least one of the embodiments of the present invention, when shifting from the first operating mode to the second operating mode, the control switching circuit part switches from the PFM control to the PWM control where the output voltage from the output terminal is equal to the first voltage.

According to at least one of the embodiments of the present invention, the switching regulator further includes a dummy load in which a predetermined electric current flows. The control switching circuit part connects the dummy load to the output terminal for a predetermined period when the output voltage from the output terminal

becomes equal to the second voltage.

According to at least one of the embodiments of the present invention, the control switching circuit part includes a PWM control circuit part performing the PWM
5 control on the first switching element, a PFM control circuit performing the PFM control on the second switching element, a switching circuit part controlling outputting control signals from each of the PWM control circuit part and the PFM control circuit part to the second control electrode of the second
10 switching element, and a control circuit part controlling operations of the PWM control circuit part, the PFM control circuit part and the switching circuit part. The control circuit part stops operations of the PWM control circuit part and directs the switching circuit part to output the control
15 signal from the PFM control circuit part exclusively to the second control electrode of the second switching element in the first operating mode. The control circuit part operates the PWM control circuit part and directs the switching circuit part to output the control signal from the PWM
20 control circuit part exclusively to the second control electrode of the second switching element in the second operating mode. The control circuit part increases the output voltage stepwise progressively from the first voltage to the second voltage where the control circuit part stops
25 the operations of the PWM control circuit part and directs

the switching circuit part to output the control signal from
the PWM control circuit part exclusively to the second
control electrode of the second switching element when
shifting the first operating mode to the second operating
5 mode.

According to at least one of the embodiments of
the present invention, the switching regulator further
includes a dummy load in which a predetermined electric
current flows. The control circuit part connects the dummy
10 load to the output terminal for a predetermined period when
the output voltage from the output terminal becomes equal to
the second voltage.

According to at least one of the embodiments of
the present invention, an electric current flowing into the
15 load in the first operating mode is smaller than the electric
current flowing into the load in the second operating mode.

According to at least one of the embodiments of
the present invention, as the voltage difference between the
first voltage and the second voltage becomes large, the
20 number of steps of increasing the output voltage stepwise
progressively from the first voltage to the second voltage is
increased in the control switching circuit part.

According to at least one of the embodiments of the
present invention, the smoothing circuit part connected to
25 the first switching element in series comprises a switching

element for synchronous rectification. The switching element
for synchronous rectification is controlled by the control
switching circuit when performing switching. The first
switching element, the second switching element, the control
5 switching circuit part, the switching element for synchronous
rectification and the dummy load are integrated into an IC.

According to at least one of the embodiments of the
present invention, the method for switching the output
voltage of the switching regulator further comprising a step
10 of switching the PFM control to the PWM control in a state
where the output voltage from the output terminal is the
first voltage when shifting from the first operating mode to
the second operating mode.

According to at least one of the embodiments of
15 the present invention, the switching regulator further
includes a dummy load in which a predetermined electric
current flows. The method further includes a step of
connecting the dummy load to the output terminal for a
predetermined period when the output voltage from the output
20 terminal becomes equal to the second voltage.

According to at least one of the embodiments of
the present invention, in the method for switching the output
voltage of the switching regulator, an electric current
flowing into the load in the first operating mode is smaller
25 than the electric current flowing into the load in the second

operating mode.

According to at least one of the embodiments of the present invention, the method for switching the output voltage of the switching regulator further comprising a step
5 of increasing the number of steps of increasing the output voltage stepwise progressively from the first voltage to the second voltage as the voltage difference between the first voltage and the second voltage becomes large.

According to the above described switching regulator,
10 the dummy load which is a pseudo load in which a predetermined electric current flows is further installed. The control switching circuit part connects the dummy load to the output terminal for a predetermined period when the output voltage from the output terminal becomes equal to the
15 second voltage. Accordingly, even if the load electric current does not increase immediately after the PFM control is shifted to the PWM control, the PWM control can be performed stably.

Further, the present invention is not limited to
20 these embodiments, but variations and modifications may be made without departing from the scope of the present invention.

The present application is based on Japanese Priority Application No.2004-342430 filed on November 26,
25 2004, with the Japanese Patent Office, the entire contents of

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which are hereby incorporated by reference.